REMARKS

The present Amendment amends claim 1 leaves claims 2-9 unchanged. Therefore, the present application has pending claims 1-9.

Applicants are submitting on even date herewith drawing corrections to Fig. 4 as per the attached Proposed Drawing Correction/Replacement Sheet. Entry and approval of the same is respectfully requested.

Claims 1-3 and 7 stand rejected under 35 USC §103(a) as being unpatentable over Kobayashi (U.S. Patent No. 6,683,642) in view of Applicants' alleged admitted prior art; and claims 4-6, 8 and 9 stand rejected under 35 USC §103(a) as being unpatentable over Kobayashi in view of Applicants' alleged admitted prior art. These rejections are traversed for the following reasons. Applicants submit that the features of the present invention as now recited in claims 1-9 are not taught or suggested by Kobayashi or Applicants' alleged admitted prior art whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections.

Amendments were made to claim 1 from which claims 2-9 depend to more clearly describe features of the present invention as recited in the claims. Particularly, amendments were made to claim 1 to recite that the present invention is directed to a video transmission apparatus for connecting to a network.

According to the present invention the video transmission apparatus includes a central processing unit block, and a peripheral block.

Further, according to the present invention the peripheral block includes a video processing unit for processing video signals from an image picking-up device and generating video data, a network control unit for controlling transmission and reception of the video data transmitted and received through a transmission medium inclusive of a network, and a first bus for providing a daisy-chain type connection such that video data output by the video processing unit is input to the network control unit, without any branch of the video processing unit and the network control unit.

Still further, according to the present invention the central processing unit block includes a central processing unit for processing the video data, a storage unit for storing video data from the video processing unit, a central control unit for controlling the video processing unit, the network control unit and the storage unit in cooperation with the central processing unit to control transmission or reception of video data in accordance with instructions from the central processing unit, and a second bus for providing a daisy-chain type connection of the central control unit, the storage unit and the central processing unit such that data received from the network control unit is output to the storage unit and video data output from the storage unit is input to the central processing unit, wherein the first bus and the second buses are connected to each other in series through a first bus buffer.

Thus, according to the present invention the daisy chain which is one type of connection system for connecting devices such as peripheral devices by cable, connects the peripheral devices in such a manner that data is transmitted by being relayed (repeated) by other peripheral devices.

The daisy chained connection is a method of connecting peripheral devices one after another in a chain fashion.

In the present invention, a series connection starts/ends at a bus buffer, which is another feature of the invention. The HD74LVVC245 product makes no clear mention of the spiral layout of components. The "spiral" layout is a layout to realize the "daisy chained connection" and hence is a feature of applicant's invention. The 7.2 Mbps transmission is not possible unless the daisy chained connection of the present invention is used. No prior art can perform in a similar manner. It should be noted that the description at p. 9, line 21 of the present application referred to by the Examiner is in fact a part of the description of an object of the present invention. Thus, this disclosure in the present application is not of the present invention but is in fact a description of the [prior art.

The present invention teaches that a start/end of a daisy chained connection is arbitrary defined using a bus buffer. The present invention features defining a start/end of a daisy chained connection with a bus buffer. The present invention is concerned with a decoding function, not troubleshooting. With the arrangement of the bus in a spiral fashion, the daisy chained connection is made possible. Therefore, the Examiner's reasoning here is irrelevant and insufficient.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, the above described features of the present invention now more clearly recited in the claims are not taught or suggested by Kobayashi or

Applicants' alleged admitted prior art whether taken individually or in combination with each other as suggested by the Examiner.

The Examiner alleges in the Office Action that Kobayashi teaches all of the features of the present invention with the exception of the network control unit. Thus, in the Office Action the Examiner readily admits that Kobayashi does not specifically disclose a network control unit for controlling transmission and reception of said video data transmitted and received through a transmission medium inclusive of a network and that the first bus provides a series connection without any branch of said video processing unit and said network control unit." (See page 4 of the Office Action) as in the present invention. In fact, providing network control unit connected in a daisy chain type connection without branch is a significant feature of the present invention not taught or suggested by Kobayashi.

The Examiner contends on page 4 of the Office Action that it would have been obvious to an ordinary skilled person to add the network control unit to Kobayashi at a location between blocks 62-60-58 and the Bus Bridge 64. However, the present invention discloses that the bus buffer defines a starting/end point of a daisy chain type connection. Such features are not taught or suggested by Kobayashi.

The Examiner further contends (see page 4-page 5) that it should be further noted that in light of Fig. 3 and the layout of the components starting from one component in a center of a chip and spiraling out to the edge of the chip may be already known, patented and commercially available (see the HD74LVVC245 product mentioned in Applicant's disclosure at page 29, lines 13-15)". Applicants do not agree. It should be pointed out that no description

of the spiral-layout is provided in the product specification of the HD74LVVC245 product. The spiral-bus layout (configuration) is a component layout (mounting) technique to realize the series (namely, daisy chain) connection and hence constitutes a feature of the present invention.

Thus, Kobayashi fails to teach or suggest the peripheral block includes a video processing unit for processing video signals from an image picking-up device and generating video data, a network control unit for controlling transmission and reception of the video data transmitted and received through a transmission medium inclusive of a network, and a first bus for providing a daisy-chain type connection such that video data output by the video processing unit is input to the network control unit, without any branch of the video processing unit and the network control unit as recited in the claims.

Further, Kobayashi fails to teach or suggest the central processing unit block includes a central processing unit for processing the video data, a storage unit for storing video data from the video processing unit, a central control unit for controlling the video processing unit, the network control unit and the storage unit in cooperation with the central processing unit to control transmission or reception of video data in accordance with instructions from the central processing unit, and a second bus for providing a daisy-chain type connection of the central control unit, the storage unit and the central processing unit such that data received from the network control unit is output to the storage unit and video data output from the storage unit is input to the central processing unit, wherein the first bus and the second buses are connected to each other in series through a first bus buffer as recited in the claims.

The above described deficiencies of Kobayashi are not supplied by the alleged admitted prior art or any of the other references of record.

The alleged admitted prior art as discussed in the Background of the Invention section of the present application has various disadvantages enumerated, for example, on page 4, lines 2-16 of the present application. These numerous disadvantages are due to the typical structure of the conventional apparatus having a plurality of dedicated bus systems are provided, wherein the dedicated bus system:

> "includes a dedicated bus that enables CPU to simultaneously and independently exchange data with the JPEG compression circuit and with the network control circuit besides a bus system through which CPU gains access to data for an execution command of CPU itself and for data to be processed".

Thus, as is quite clear from the above, the conventional apparatus, such as that taught in the Background of the Invention section of the present application, provides for a plurality of dedicated buses which in effect connect the various elements including the JPEG compression circuit (video processing unit), network control circuit and storage unit in parallel to the CPU, accomplishing the simultaneous and independent operation discussed therein. Therefore, the Background of the Invention section of the present application teaches a conventional apparatus which provides for a parallel connection of the various elements rather than a series connection as now more clearly recited in the claims.

Thus, the alleged admitted prior art, the same as Kobayashi fails to teach or suggest the peripheral block includes a video processing unit for processing video signals from an image picking-up device and generating

video data, a network control unit for controlling transmission and reception of the video data transmitted and received through a transmission medium inclusive of a network, and a first bus for providing a daisy-chain type connection such that video data output by the video processing unit is input to the network control unit, without any branch of the video processing unit and the network control unit as recited in the claims.

Further, the alleged admitted prior art, the same as Kobayashi fails to teach or suggest the central processing unit block includes a central processing unit for processing the video data, a storage unit for storing video data from the video processing unit, a central control unit for controlling the video processing unit, the network control unit and the storage unit in cooperation with the central processing unit to control transmission or reception of video data in accordance with instructions from the central processing unit, and a second bus for providing a daisy-chain type connection of the central control unit, the storage unit and the central processing unit such that data received from the network control unit is output to the storage unit and video data output from the storage unit is input to the central processing unit, wherein the first bus and the second buses are connected to each other in series through a first bus buffer as recited in the claims.

Therefore, since each of Kobayashi and Applicants' alleged admitted prior art fails to teach or suggest the features of the present invention as now more clearly recited in the claims, the combination of Kobayashi and Applicants' alleged admitted prior art does not render obvious the claimed invention. Accordingly, reconsideration and withdrawal of the 35 USC §102(e) rejection of claims 1-3 and 7 as being unpatentable over Kobayashi

and Applicants' alleged admitted prior art and reconsideration and withdrawal of the 35 USC §103(a) rejection of claims 4-6, 8 and 9 as being unpatentable over Kobayashi and Applicants' alleged admitted prior art are respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of claims 1-9.

In view of the foregoing amendments and remarks, applicants submit that claims 1-9 are in condition for allowance. Accordingly, early allowance of claims 1-9 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (500.41299X00).

Respectfully submitted,

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